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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2188	

MAIL DATE	DELIVERY MODE
12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,438	PARTSCH, TORSTEN	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-38 are pending in the Application.

Response to Amendment

2. Applicant's arguments filed on 25 September 2007 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 17, 18, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Usami (US Patent No. 6,205,516).

5. **Regarding Claims 1 - 3, 17, 18, and 31,** Usami discloses a random access memory, comprising: an array of memory cells; a memory configured to receive data from the array of memory cells; a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to

provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency signal. Also, the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency signal indicates a column address strobe latency value of one. Lastly, when the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one. **(See Figure 2 and Figure 4)**

6. **Usami discloses a programmable SDRAM. An SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS Latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. Usami teaches varying the CAS Latency (CL) from at least CL-1 to CL-3. Having a CL-1 means that there is one pipeline stage, meaning the data is sent directly to the memory. While**

a CL-3 means that there are three pipeline stages, meaning the data is sent through multiple pipeline stages before being sent to the memory. Applicant has stated that Usami teaches controlling the CAS Latency based on controlling the column address counter, thereby controlling count up timing and count up number of the column address timer. While this count up timing is taking place, the data is being stalled, which will appropriately adjust the CAS Latency to the one desired. As is common in pipelines, a stall in this instance is equivalent to one stage of the pipeline. Therefore, even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-16, 19-30 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (US Patent No. 6,205,516).

9. **Regarding Claims 4-11, 19-21, 25-30, and 33-38,** Usami discloses circuits configured to receive first rise and fall signals to serialize the data following a read command initiated by an edge of a clock cycle. **(See Figures 2 and 4.)**

10. **A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. Using Fetterman et al. ((US Patent No. 5,553,256) herein after Fetterman) and Sharma et al. ((US Patent No. 5,829,016) herein after Sharma), as evidentiary support, the limitations are taught. Fetterman (Column 15, Lines 9-14) teaches a read command which coincides with the rising edge of a clock cycle. While Sharma (Column 10, Lines 19-21) teaches a read command which begins on the falling edge. Therefore either rising or falling clock edges can be used to provide an instruction to receive data.**

11. **Regarding Claims 12-16, 22-24, and 32,** Usami fails to disclose a tri-state output, a first in/first out memory, a low power synchronous dynamic random access memory, a double data rate-I synchronous dynamic random

access memory, a double data rate-II synchronous dynamic access memory, a data delay circuit, and an off chip driver.

However, it would have been obvious for a person of ordinary skill in the art to combine these limitations with the random access memory of Usami.

The motivation for doing so would have been that using tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, and off chip drivers in random access memory devices is an efficient way to utilize system resources along with expediting memory requests.

Therefore it would have been obvious for a person of ordinary skill in the art to combine the use of tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, or off chip drivers with the random access memory of Usami, for the benefit of efficiently utilizing system resources along with expediting memory requests to obtain the invention claimed.

A tri-state output is taught using Cochran (US Patent No. 3,958,223) as evidentiary support. (Cochran: Column 11, Lines 64-68.) A first in/first out memory is taught by Altman (US Patent No. 3,593,286).(Altman: Column 9, Lines 73-75). A low power synchronous random access memory, otherwise known as low power SDRAM, is taught by Bunker (US Patent No. 6,469,474.)(Bunker: Column 8, Lines 54-56) A double data rate-I synchronous dynamic random access memory, otherwise known as DDR-I SDRAM, is taught by Tien et al ((US Patent No. 5,923,613) herein after Tien.)(Tien: Column 3, Lines 55-58.) A double data rate-II synchronous dynamic random access memory, otherwise known as a DDR-II SDRAM, is

taught by Hovis et al. ((US Patent No. 6,434,082) herein after Hovis.)(Hovis: Column 7, Line 60 – Column 8, Line 16.) A data delay circuit is taught by Benowitz et al. ((US Patent No. 3,614,317) herein after Benowitz)(Benowitz: Column 4, Lines 60-63.) An off chip driver is taught by Cox et al. ((US Patent No. 3,987,287) herein after Cox)(Cox: Column 7, Lines 12-25.) The respective limitations have been taught using the sited patents as evidentiary references.

12. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (US Patent No. 6,205,516) and further in view of Sakamoto et al. (("A Digitally Programmable Delay Chip with Picosecond Resolution") herein after Sakamoto).

13. For the purposes of the following rejection Usami fails to disclose a bypass circuit.

14. **Regarding Claims 1 - 3, 17, 18, and 31,** Usami and Sakamoto disclose a random access memory, comprising: an array of memory cells; a memory configured to receive data from the array of memory cells; a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency signal. Also, the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second

output signals if the column address strobe latency signal indicates a column address strobe latency value of one. Lastly, when the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one. **(Usami: Figure 2 and Figure 4.) Usami discloses a programmable SDRAM. An SDRAM is inherently created from a memory array, a memory configured to receive data from the array, and a circuit that will select the programmed mode. Usami: Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS Latency) will vary accordingly as described in Claims 2 and 3. Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline stage, a bypass circuit and a circuit configured to select between receiving data are inherent. Usami teaches varying the CAS Latency (CL) from at least CL-1 to CL-3. Having a CL-1 means that there is one pipeline stage, meaning the data is sent directly to the memory. While a CL-3 means that there are three pipeline stages, meaning the data is sent through multiple pipeline stages before being sent to the memory. Applicant has stated that Usami teaches controlling the CAS Latency based on controlling the column address counter, thereby controlling**

count up timing and count up number of the column address timer. While this count up timing is taking place, the data is being stalled, which will appropriately adjust the CAS Latency to the one desired. As is common in pipelines, a stall in this instance is equivalent to one stage of the pipeline. Therefore, even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether.

15. **To further clarify, a delay circuit is taught by Sakamoto. Sakamoto: Figure 1 shows delay circuitry that receives an input and will then delay the data by use of a chain of multiple buffers. As previously stated, if CL-3 then it will need to be delayed three pipeline stages. This will happen by use of the delay circuit. The input will go into the 32 to 1 multiplexer and through the delay chain of buffers as necessary until the desired delay is achieved. However, when CL-1 is selected there can be no delay. The input will go into the 32 to 1 multiplexer and will immediately be outputted. Therefore at the very least the delay chain of buffers will be bypassed. Therefore the combination of Usami and Sakamoto discloses a bypass circuit.**

16. Usami and Sakamoto are analogous art because they are from the same field of endeavor, digital circuits involving delay circuitry.

17. At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the delay circuitry of Sakamoto as the counter delay in Usami.

18. The motivation for doing so would have been achieving high performance and providing low power dissipation.

19. Therefore it would have been obvious to utilize the delay circuitry of Sakamoto as the counter delay in Usami for the benefit of achieving high performance and providing low power dissipation to obtain the invention as specified in claim 1.

20. **Regarding Claims 4-11, 19-21, 25-30, and 33-38,** Usami and Sakamoto disclose circuits configured to receive first rise and fall signals to serialize the data following a read command initiated by an edge of a clock cycle. **(Usami: Figures 2 and 4.)**

21. **A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed. Using Fetterman et al. ((US Patent No. 5,553,256) herein after Fetterman) and Sharma et al. ((US Patent No. 5,829,016) herein after Sharma), as evidentiary support, the limitations are taught. Fetterman (Column 15, Lines 9-14) teaches a read command which coincides with the rising edge of a clock cycle. While Sharma (Column 10, Lines 19-21)**

teaches a read command which begins on the falling edge. Therefore either rising or falling clock edges can be used to provide an instruction to receive data.

22. **Regarding Claims 12-16, 22-24, and 32,** Usami and Sakamoto fail to disclose a tri-state output, a first in/first out memory, a low power synchronous dynamic random access memory, a double data rate-I synchronous dynamic random access memory, a double data rate-II synchronous dynamic access memory, a data delay circuit, and an off chip driver.

However, it would have been obvious for a person of ordinary skill in the art to combine these limitations with the random access memory of Usami.

The motivation for doing so would have been that using tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, and off chip drivers in random access memory devices is an efficient way to utilize system resources along with expediting memory requests.

Therefore it would have been obvious for a person of ordinary skill in the art to combine the use of tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, or off chip drivers with the random access memory of Usami, for the benefit of efficiently utilizing system resources along with expediting memory requests to obtain the invention claimed.

23. **A tri-state output is taught using Cochran (US Patent No. 3,958,223) as evidentiary support. (Cochran: Column 11, Lines 64-68.) A first in/first out memory is taught by Altman (US Patent No. 3,593,286).(Altman: Column 9, Lines 73-75). A low power synchronous random access memory,**

otherwise known as low power SDRAM, is taught by Bunker (US Patent No. 6,469,474.)(Bunker: Column 8, Lines 54-56) A double data rate-I synchronous dynamic random access memory, otherwise known as DDR-I SDRAM, is taught by Tien et al ((US Patent No. 5,923,613) herein after Tien.)(Tien: Column 3, Lines 55-58.) A double data rate-II synchronous dynamic random access memory, otherwise known as a DDR-II SDRAM, is taught by Hovis et al. ((US Patent No. 6,434,082) herein after Hovis.)(Hovis: Column 7, Line 60 – Column 8, Line 16.) A data delay circuit is taught by Benowitz et al. ((US Patent No. 3,614,317) herein after Benowitz)(Benowitz: Column 4, Lines 60-63.) An off chip driver is taught by Cox et al. ((US Patent No. 3,987,287) herein after Cox)(Cox: Column 7, Lines 12-25.) The respective limitations have been taught using the sited patents as evidentiary references.

Response to Arguments

24. Applicant's arguments filed on 25 September 2007 have been fully considered but they are not persuasive.

25. **Regarding Claims 1, 17, 18, and 31,** Applicant contends that there is not a single reference to a cache memory including pipeline stages in Usami. **However, when discussing CAS Latency, it is inherent that you are referring to pipeline stages. That is how CAS Latency is measured, in pipeline stages. As previously stated in the rejection, a CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, by providing various CAS Latencies, it is inherent**

that Usami teaches pipeline stages. Applicant also contends a bypass circuit is not inherent to Usami and that varying the CAS latency in Usami could be performed without utilizing a bypass circuit. **However, Usami teaches varying the CAS Latency (CL) from at least CL-1 to CL-3. Having a CL-1 means that there is one pipeline stage, meaning the data is sent directly to the memory. While a CL-3 means that there are three pipeline stages, meaning the data is sent through multiple pipeline stages before being sent to the memory. Applicant has stated that Usami teaches controlling the CAS Latency based on controlling the column address counter, thereby controlling count up timing and count up number of the column address timer. While this count up timing is taking place, the data is being stalled, which will appropriately adjust the CAS Latency to the one desired. As is common in pipelines, a stall in this instance is equivalent to one stage of the pipeline. Therefore, even though a counter is being used the data to be sent to the memory is being stalled in a buffer. In order to achieve a CL-1 then this buffer must be bypassed altogether. Therefore, a bypass circuit, in some form, must inherently be present.**

26. **Regarding Claim 8,** Applicant contends that Usami fails to teach wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal. **However, Usami teaches that the CAS Latency is determined based on the CAS Latency bits of Figure 4. The mode register is this sense functions as the multiplexer by taking the**

control signal (the latency bits) and interpreting it to determine between the bypassing of the stall buffer or not.

27. **Regarding the 103 rejection of Claim 1,** the Applicant contends that Sakamoto fails to disclose a bypass circuit. **However, as stated in the rejection Sakamoto is relied upon to teach a delay circuit. That delay circuit is used as the delay counter.** The Applicant contends Usami fails to disclose a delay counter and therefore one skilled in the art could not combine Usami and Sakamoto. **Usami discloses a memory with a programmable CAS latency. Usami uses a counter to introduce the delay, as needed, into the circuit to add pseudo-pipeline stages. Therefore, Usami does disclose a delay counter.**

28. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above. Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sam Sough can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBM
12/09/2007

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
12/10/07